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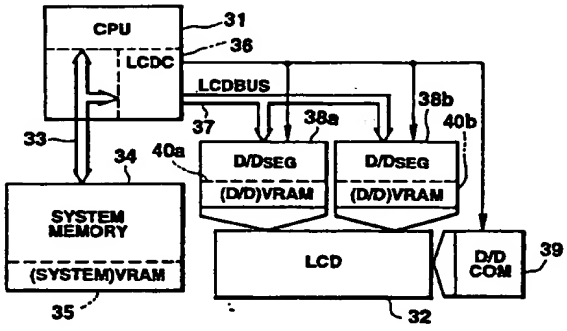
(54) Display data write control device.

(57) A system memory (34) in the electronic device has a display data memory area (35), and when a CPU (31) accesses directly to the system memory (34), the liquid crystal display control section (LCDC) (36) monitors whether or not address data is directed to the display data memory area (35). In the case where the address data is directed to the display memory area (35), the LCDC (36) transfers display data and address data to the display driving circuit (38a, 38b). The display driving circuit (38a or 38b) comprises a VRAM (40a or 40b), in which the display data is stored in a predetermined memory location in accordance with the received address data, and the stored data is displayed on the LCD (32).

FIG.1



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(54) Display data write control device.

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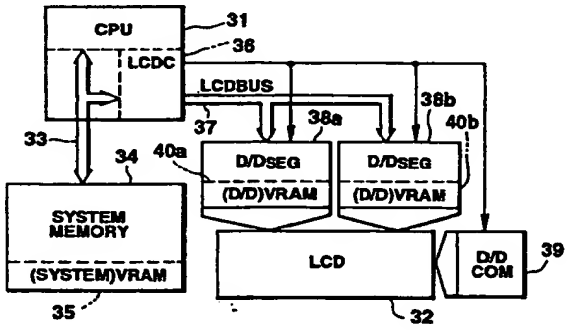
FIG.1



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The present invention relates to a control device for writing display data in a memory, which is used, for example, in an electronic device having a liquid crystal display section.

FIG. 5 is a diagram showing the structure of a conventional display control device having a display video memory (VRAM) in a system memory. The system memory 13 is connected to a central processing unit (CPU) 11 via data and address bus 12, and also segment display drivers (D/D_{SEG}) 15a and 15b of a dot matrix liquid crystal display 14 are connected to the CPU 11.

The CPU 11 includes a liquid crystal display control section 11a, control signals from which are supplied to the system memory 13, D/D_{SEG} 15a and 15b, as well as to a common display driver (D/D_{COM}).

In the conventional display control device shown in FIG. 5, the VRAM 13a is provided in the system memory 13, and the VRAM 13a in the system memory 13 is directly accessed by the CPU 11 for writing/reading of data to be displayed. Therefore, the software burden can be reduced. However, while data being displayed on the LCD 14, the display data in the VRAM 13a must be transferred at all times to the D/D_{SEG} 15a and 15b, and therefore when the number of display pixels is increased, the data transfer amount, that is, the number of times of data access to the VRAM 13a, is accordingly increased, resulting in consuming a great amount of current.

FIG. 6 is a diagram showing the structure of another conventional display control device comprising a display video memory (VRAM) in a display driver chip. As shown in the figure, a system memory 23, a liquid crystal display section 24, and segment display drivers (D/D_{SEG}) 25a and 25b are connected to a CPU 21 via data and address bus 22.

Display data and a write control signal for VRAMs 26a and 26b respectively provided in the D/D_{SEG} 25a and 25b are supplied to the D/D_{SEG} 25a and 25b from the CPU 21, and a display timing signal from a liquid crystal display control section (LCDC) 27 provided in the D/D_{SEG} 25a is supplied to the D/D_{SEG} 25b and a D/D_{COM} (common display driver) 28.

More specifically, in the conventional display control device shown in FIG. 6, while data being displayed on the LCD 24, a segment of the LCD 24 is driven directly by the bit pattern data written in the VRAMs 26a and 26b in the D/D_{SEG} 25a and 25b, and therefore even if there are a great number of display pixels, the number of times of data access with respect to the CPU 21 can be kept small. Further, since a multi-bit output memory can be used as a memory for display, the current consumed can be made small.

However, when the number of system buses 22 from the CPU 21 to the D/D_{SEG} 25a and 25b is reduced in designing for the purpose of the downsizing of device, the accessing of the CPU 21 to the D/D_{SEG} 25 in terms of processing of command, address and display must be carried out by software control. As a result, this display control device entails the problem of a heavy software designing burden as compared to the conventional display control device comprising the VRAM in the system memory, shown in FIG. 5.

In short, one type of the conventional display control devices has the problem of a large consuming current due to the data access to the VRAM 13a in the system memory, and the other type has the problem of a heavy software burden due to the data access with respect to the CPU 21.

The present invention has been proposed in consideration of the above problems, and the object thereof is to provide a display control device in which the software designing burden in order for storing display data output from the CPU into the display memory, can be reduced.

According to the present invention, there is provided an electronic device comprising: a dot matrix type display screen; a display driving circuit for driving the display screen; a process unit for controlling operation of the electronic device; a system memory having a memory area directly address-controllable by the process unit and containing a display memory area; and a display data write control circuit, included in the process unit, for detecting display data written from the process unit to the display memory area of the system memory, and transferring the display data to the display driving circuit.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a block diagram showing the structure of a display control device according to one embodiment of the present invention;

FIG. 2 is a block diagram showing details of a liquid crystal display controller shown in FIG. 1;

FIG. 3 is a block diagram showing details of a multiplexer of FIG. 2;

FIG. 4A is a diagram showing the structure of a VRAM of a system memory shown in FIG. 1;

FIG. 4B is a diagram showing the structure of a VRAM of a display driver shown in FIG. 1; and

FIGS. 5 and 6 are block diagrams each showing a conventional circuit.

An embodiment of the present invention will now be described with reference to drawings.

FIG. 1 is a block diagram showing the structure of a display control device of the embodiment according to the present invention.

A central processing unit (CPU) 31 serves to generate display data to a liquid crystal dot matrix display section (LCD) 32, and control the operation of each section of the device. To the CPU 31, a system memory 34 is connected via system bus 33 including data bus and address bus.

The system memory 34 comprises a video memory (VRAM) 35, in which display data transferred from the CPU 31, which is to be displayed on the LCD 32, is stored.

Inside the CPU 31, there is provided a liquid crystal display control section (LCDC) 36 connected to the system bus 33. Display data and the address data thereof output from the LCDC 36 are transferred to segment display drivers (D/D_{SEG}) 38a and 38b via a liquid crystal display bus (LCDBUS) 37, whereas a display control signal output from the LCDC 36 is supplied to the D/D_{SEG} 38a and 38b and a common display driver (D/D_{COM}) 39.

The D/D_{SEG} 38a and 38b comprise display VRAMs 40a and 40b, respectively, and the LCD 32 is driven in accordance with the display data written in the display VRAMs 40a and 40b as a bit map pattern.

FIG. 2 shows a section related to the LCDC 36 in the display control device. The address bus 33a, data bus 33b, and a R/W (read/write) control signal line 41 from a memory interface section 31a of the CPU 31 are connected to the system memory 34 and the LCDC 36 in a similar manner.

The LCDC 36 operates such that the display and address data is fetched in the multiplexer 36a when data is written from the CPU 31 to the system memory 34, and it is judged as to whether or not the data is to be written in the VRAM 35 of the system memory 34 on the basis of the address data. When the display data is to be written in the VRAM 35, the display data and the address data thereof fetched in the multiplexer 36a are transferred to the D/D_{SEG} 38a and 38b in order via the LCDBUS 37 in the time divisional manner.

FIG. 3 shows the details of the multiplexer 36a.

The multiplexer 36a includes an address calculation circuit 52 having a latch-A 51 for temporarily holding address data from the address bus 33a, and a latch-D 53 for temporarily holding the display data from the data bus 33b.

In the embodiment, the address bus 33a is made of a 20-bit type, and the data bus 33b is made of an 8-bit bus.

The address bus 33a is connected to a decoder 54. The decoder 54 serves to decode the upper 4 bits of address data, and output a signal S when the address data accesses to the VRAM 13a of the system memory 13.

Upon reception of the signal S, a selector 55 serves to output address and display data to the LCDBUS 37 in the time divisional manner. The LCDBUS 37 consists of 8-bit bus, and lower 16 bits of the address data is divided into the lower 1 byte data "AX" and the upper 1 byte data "AY".

It should be noted that the point of division of the address data determines the point of division in the X direction (the number of bytes in the X direction) of the memory area of the VRAM 35 of the system memory 34 as shown in FIG. 4A, and the significant bit number for the "AX" is not necessary 8 bits.

A DXA register 56 and a DYA register 57 serve to store "DXA" and "DYA", respectively, each of which is an amount of displacement resulted from addition to or subtraction from the address data stored in the latch-A 51.

The relationship between the LCD 32 and the VRAMs 40a, 40b will now be described.

The LCD 32 has a display screen consisting of display pixels arranged such that there are 160 dots in the vertical (Y) direction and 256 dots in the horizontal (X) direction.

Each of the VRAMs 40a and 40b provided respectively in the segment drivers (D/D_{SEG}) 38a and 38b has a memory capacity of 160 x 128 dots, and serves to store display data to be displayed on the screen, in a two-division manner.

The lower byte data "AX" of the address data serves to designate the selection of two segment drivers (D/D_{SEG}) 38a, 38b and the address of the VRAM in the X direction, whereas the upper byte data "AY" serves to designate the address in the Y direction.

The VRAM area 35 of the system memory 34 has a capacity larger than the total capacity of the VRAM 40a and VRAM 40b of the segment drivers (D/D_{SEG}), and includes the display data memory area corresponding to the VRAMs 40a, 40b of the segment drivers (DD_{SEG}).

The LCDC 36 includes a direct memory access circuit (DMA) 58, a display timing control section 36b and read/write control section 36c operating as a data collision avoidance control section.

When start address (S), the number of bytes (x) in the X direction and the number of bits (y) in the Y direction are set by the CPU 31, the DMA 58 automatically reads data having a rectangular area of $x \cdot y$ with respect to start address S as the starting point, from the VRAM area 35 of the system memory 34, and write the data into the VRAM 40a or 40b of the segment driver (DD_{SEG}) 38a or 38b.

The display timing control section 36b serves to output a display timing signal necessary to drive the LCD 32 to each of the segment drivers (D/D_{SEG}) 38a and 38b and the common driver (D/D_{COM}) 39. In reply to the display timing signal, the common driver (D/D_{COM}) outputs a common signal, whereas each of the segment drivers (D/D_{SEG}) 38a and 38b

outputs a segment signal in accordance with the display bit map data stored in the VRAMs 40a and 40b.

The read/write control section 36c functioning as the data collision avoiding control section serves to avoid the data write timing for the VRAMs 40a, 40b of the segment drivers (D/D_{SEG}) 38a and 38b overlapping with the data read timing for display on the LCD 32, and output a collision avoiding control signal on the basis of the timing control operation for the LCD 32 by the display timing control section 36b and the data write control signal output from the CPU 31.

The operation of the embodiment will now be described.

In the case where the CPU 31 operates to write display data to be displayed on the LCD 32 in the VRAM 35 of the system memory 34, a write signal is output to the R/W signal line 41, and the address and display data are output to the address and display buses 33a and 33b, respectively. Then, the display data is written in the system memory 34 in accordance with the address data.

In the LCDC 36, the address data is stored in the latch-A 51, whereas the display data is stored in the latch-D 53. At the same time, in the decoder 54, it is judged as to whether or not the address data addresses the VRAM area 35 of the system memory 34.

When it is judged that the address data addresses the VRAM area 35 of the system memory 34, the display data and the address data are time-division-output to the LCDBUS 37. More specifically, the selector 55 selectively outputs the lower byte "AX" of the address data, the upper byte "AY" stored in the latch-A 51, and the display data "DD" stored in the latch-D 53 to the LCDBUS 37 in order. The display segment drivers (D/D_{SEG}) 38a, 38b receives these data, and write the display data to a designated VRAM 40a or 40b.

The display data written in the VRAMs 40a and 40b of the segment drivers (D/D_{SEG}) 38a and 38b are read out based on the display timing signal output from the display timing control section 36b of the LCDC 36, and sent to the segment electrodes in the LCD 32. The display data is then synchronized with the common signal output from the common driver (D/D_{COM}) 39, and thus the LCD 32 is driven.

Next, the case where a window is opened on the display screen of the LCD 32 so as to display other display data in a portion of the background display data, will now be described.

Let us suppose the case as shown in FIG. 4B, for example, in which window data is written from the point where the address is displaced by "bx" in the X direction and "by" in the Y direction with respect to the original address (the upper left corner of the screen of FIG. 4B) of the VRAM memory area of the segment driver, which corresponds to the LCD 32.

Window display data is written in a memory area other than the area where the display data presently displayed is stored, within the entire area of the VRAM 35 of the system memory 34, by the CPU 31. FIG. 4A illustrates data stored in the VRAM 35 in a visualized form, and the region defined by the broken lines indicates a memory area for display data. Suppose that the window display data is written to the shaded area of FIG. 4A, and the write start address thereof is set at "ax" and "ay". Then, the CPU 31 determines the values of "DXA" and "DYA" such as to satisfy the following equations:

$$ax + DXA = bx$$
$$ay + DYA = by$$

and sets the determined values to the DXA register 56 and DYA register 57, respectively. Then, the address calculation circuit 52 calculates out "AX" data by adding the "DXA" and the lower byte of the address data stored in the latch-A 51 and "AY" data by adding the "DYA" and the upper byte, and outputs the obtained "AX" and "AY" data to the segment drivers (D/D_{SEG}) 38a, 38b via the selector 55. The segment driver 38a or 38b stores the display data into the VRAM 40a or 40b in accordance with the address data received.

Consequently, when window data is written in by addressing a certain area in the VRAM 35 of the system memory 34, the address data and display data are transferred to the segment drives 38a and 38b via the LCDC 36, and a window is automatically displayed on the LCD 32 at the designated location.

In such an operation, as shown in FIG. 4A, the display data for the background image and that for the window are stored in different areas of the system VRAM 35, and therefore, even if a window is superimposed over a part of of the current image, it is not necessary to save the background image data of the area corresponding to the location of the window.

Moreover, by utilizing the function of the DMA 58, the window display data written in the VRAM 35 of the system memory 34 and the portion of the background image data hidden behind the window can be written in the VRAM 40a or 40b of the segment driver 38a or 38b, thereby simplifying the display of a window and the recovering operation of the background image. In the case where the display data is read by the CPU 31, the data is read out directly from the system memory 34, and the LCDC 36 does not operate.

With the present invention having the abovedescribed structure, developers of software have to consider only direct access to the VRAM in a system memory as regards the display data write process, and therefore the software designing burden can be reduced.

Lastly, the present invention is not limited to the embodiments described above, and can be modified into a variety of version without departing from the scope thereof.

Claims

1. An electronic device characterized by comprising:
   a dot matrix type display screen (32);
   a display driving circuit (38a, 38b, 39) for driving said display screen;
   a process unit (31) for controlling operation of said electronic device;
   a system memory (34, 35) directly addressed by said process unit and containing a display memory area (35); and
   a display data write control circuit (36), included in said process unit (31), for detecting display data written from said process unit (31) to said display memory area (35) of said system memory, and transferring the display data to said display driving circuit (38a, 38b).

2. An electronic device according to claim 1, characterized in that said display driving circuit has an image memory (40a, 40b) corresponding to said display screen (32).

3. An electronic device according to claim 2, characterized in that said display data write control circuit includes means (54) for judging whether or not address data supplied to said system memory is to address said display area by decoding said address data.

4. An electronic device according to claim 3, characterized in that said display data write control circuit includes transferring means (55) for transferring said display data and said address data to said display driving circuit.

5. An electronic device according to claim 4, characterized in that said display screen includes a liquid crystal display device (32), and said display driving circuit includes a segment drive circuit (38a, 38b) having said image memory and a common signal generating circuit (39).

6. An electronic device according to claim 5, characterized in that said display data write control circuit includes a direct memory access controller (58) for transferring data in said display memory area (35) of said system memory to said image memory.

7. An electronic device according to claim 5, characterized in that said display data write control circuit includes means (51, 56, 57) for varying said address data by a predetermined displacement amount and transferring the varied address data to said display driving circuit.

8. A display device characterized by comprising:
   display means (32), having a display screen, for displaying display data;
   first memory means (40a, 40b) for storing the display data displayed on said display screen;
   second memory (34) having a memory area (38) a predetermined part of which is determined as a display data storing area;
   write means (31) for writing the display data in said second memory means;
   detection means (36) for detecting that a data writing operation by said write means is directed to said display data storing area of said second display means; and
   write control means (36) for controlling writing of said display data in said first memory means when the data writing operation of said display data is detected by said detection means.

9. A display device according to claim 8, characterized in that said write means (31) further includes means for supplying said address data and said display data in said second memory means, and said detection means (36) further includes means (54) for judging whether or not said address data is directed within a certain range corresponding to said display data storing area.

10. A display device according to claim 9, characterized in that said first memory means (40a, 40b) is included in a display driving circuit.

11. A display device according to claim 10, characterized in that said display screen of said display means includes a liquid crystal display screen (38), and said display driving circuit has a segment driver (38a, 38b) for said liquid crystal display screen.

12. A display device according to claim 10, characterized in that said write control means (36) further includes transfer means (55) for transferring said display data and address data to

said display driving circuit, and said display driving circuit includes means for writing said transferred display data in said first memory means on the basis of said address data transferred by said transfer means.

13. A display device according to claim 12, characterized in that said write control means further includes operation means (51) for adding or subtracting a predetermined value to or from said address data.

14. A display memory control means characterized by comprising:

a display screen (22);

a display driving circuit (38a, 38b) for driving said display screen;

first memory means (40a, 40b), included in said display driving circuit and addressed by two types of address data as for X and Y directions, for storing display data corresponding to said display screen;

second memory means (24, 35) directly accessed by a CPU (31), said second memory means having an area (35) not less than that of said first memory means, for storing the display data;

third memory means (56, 57) for storing a displacement amount value;

address data processing means (52) for adding or subtracting said displacement amount value stored in said third memory means to or from said address data when the CPU carries out a write operation to said second memory means; and

control means (36a) for outputting said address data processed by said address data processing means to said first memory means.

15. A display memory control device according to claim 14, characterized by further comprising judging means (54) for judging whether or not said area of said second memory means for storing the display data is to be accessed.

16. A display memory control device according to claim 15, characterized in that said address data contains upper bit data indicating an X addressing direction and lower bit data indicating a Y addressing direction, and said third memory means includes means (56, 57) for storing said displacement amount value of each of the X and Y direction components.

17. A display memory control device according to claim 14, characterized in that an address of a first memory area of said display data storing area of said second memory means corresponds to an address of a second memory area of said first memory means, and said display memory control device further comprises means (52) for addressing an area other than the display data storing area of said second memory means to store window data, means (31, 56, 57) for setting a displacement amount value to said third memory means to write window display data to a predetermined memory location of said first memory means and means for displaying a window in accordance with the window display data.

18. A display memory control device according to claim 14, characterized in that said display screen (32) includes a liquid crystal display device, and said first memory means (38a, 38b) is included in a segment driver chip.

FIG.3

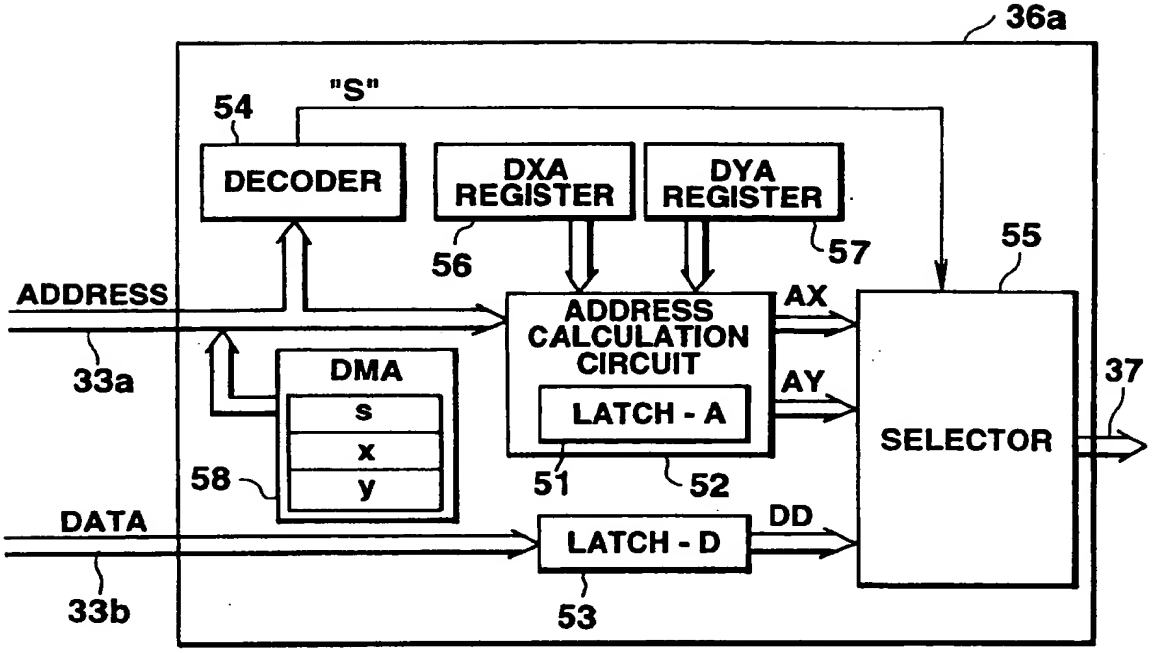

FIG.4A

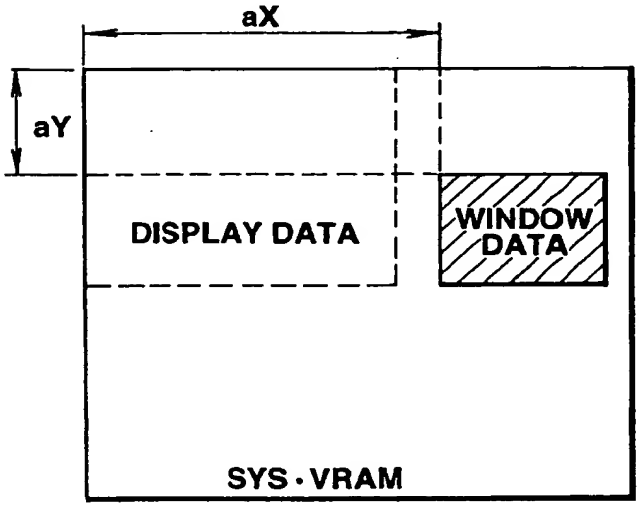

FIG.4B

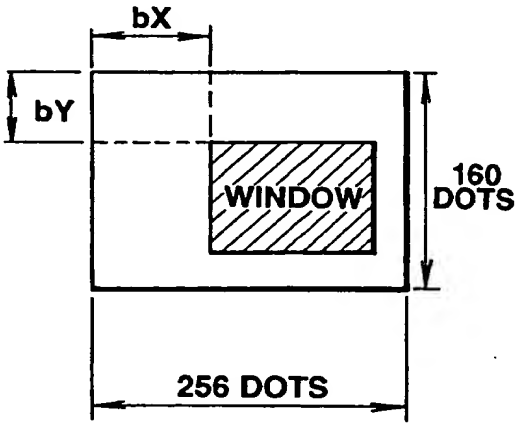

FIG.5
PRIOR ART

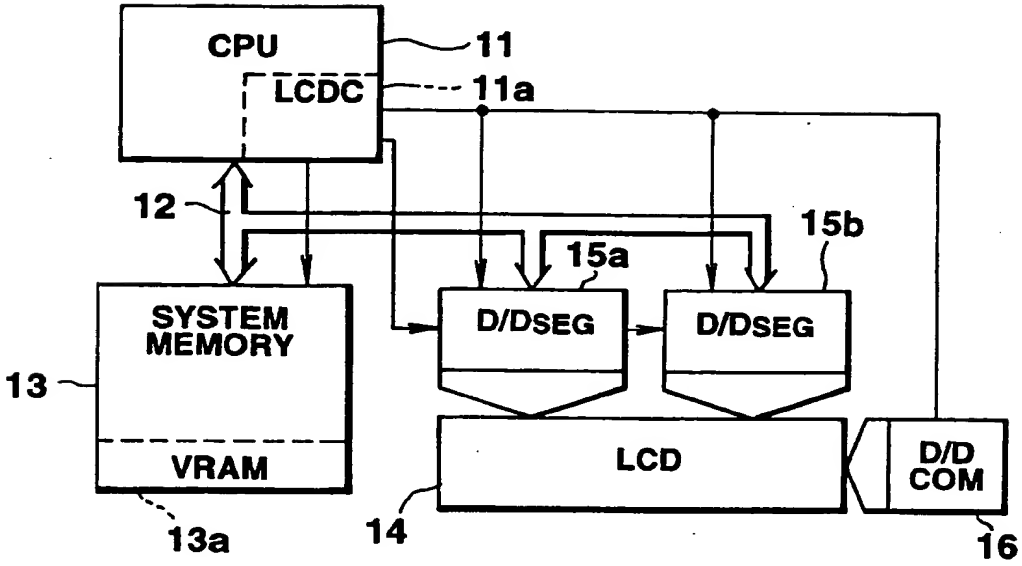

FIG.6
PRIOR ART

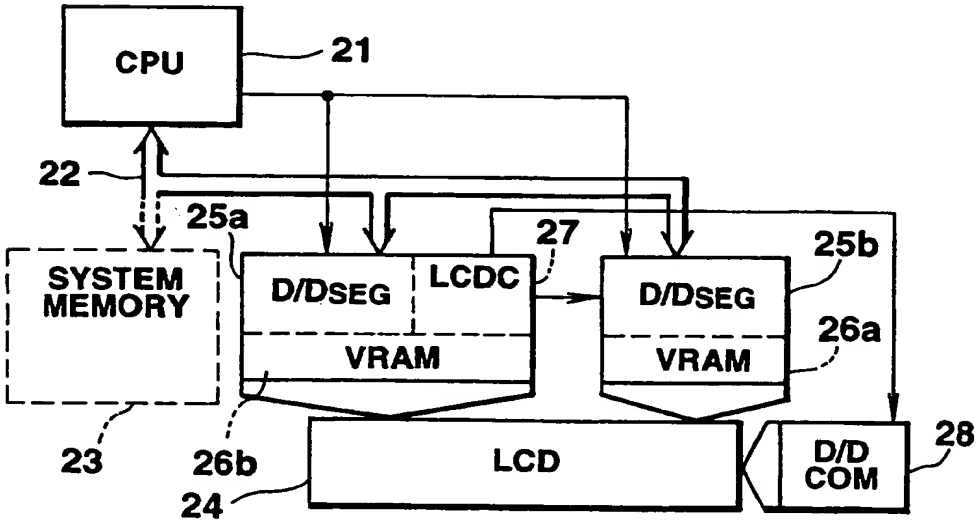

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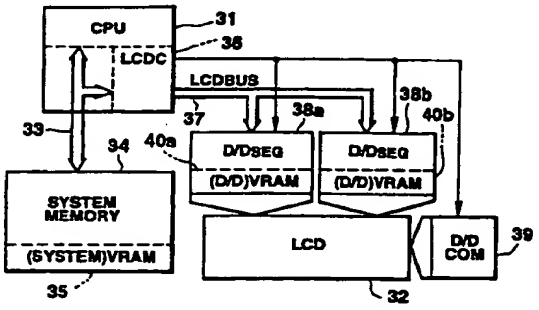
FIG.1



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European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 94 10 2672

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
A	EP 0 172 055 A (TEXAS INSTRUMENTS FRANCE) * abstract * * page 2, line 18 - line 20 * * page 3, line 24 - page 4, line 18 * * page 6, line 25 - page 7, line 4 * * page 7, line 26 - page 8, line 4; figures 1-3,5-9 *	1-13	G09G3/36
A	EP 0 411 464 A (KABUSHIKI KAISHA TOSHIBA) * abstract * * column 2, line 27 - column 3, line 9; figures 1,2 *	1-13	
A	EP 0 482 263 A (ACER INC.) * abstract * * column 2, line 10 - line 51; figure 3 *	1-13	
X	GB 2 215 959 A (BENCHMARK TECHNOLOGIES LTD.)	14,17	
A	* abstract * * page 8, line 2 - line 10 * * page 13, line 12 - line 16 * * page 45, line 25 - page 47, line 12; figures 1,5 *	15,16,18	

TECHNICAL FIELDS SEARCHED (Int.Cl.5)

G09G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	4 April 1997	O'Reilly, D

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